Publication number:

212328

ø

EUROPEAN PATENT APPLICATION

Application number: 86110247.3

6505668042

Date of filing: 25.07.86

60 Int. Cl.4: H 01 L 29/68, H 01 L 33/00

Priority: 26.07,85 US 759634 17.10.85 US 788594

1675 West Maple Road, Troy Michigan 48084 (US)

Applicant: ENERGY CONVERSION DEVICES, INC.,

- Date of publication of application: 04.03.87 Bulletin 87/10
- Inventor: Czubatyj, Wolodymyr, 2426 Walter, Warren Michigan 48092 (US) Inventor: Hack, Michael G., 1225 Kenilworth, Clawson Michigan 48017 (US) inventor: Shur, Michael, 217 Janalyn Circle, Golden Valley Michigan 55416 (US)
- Designated Contracting States: AT BE CH DE FR GB [T L] LUNLSE
- Representative: Müller, Hans-Jürgen, Dipt.-ing. et al, Müller, Schupfner & Gauger Lucile-Grahn-Strasse 38 Postfach 80 13 69, D-8000 München 80 (DE)

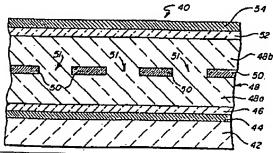
Double injection field effect transistor.

ന

A field effect transistor (FET), which may be horizontally or vertically arranged, includes a body of semiconductor material extending between two current-carrying electrodes and forming a current path therebetween. Some embodiments are thin film devices; others are crystalline devices. Some have a semiconductor body that is substantially intrinsic; others have a semiconductor body that is doped. A control electrode or gate located adjacent to the current path projects a variable electric field over the path. which modulates current by controlling the amount of charge carriers injected into the semiconductor body. The preferred embodiments are double injection FETs, called DIFETs, which have ambipolar current in the current path and thus exhibit increased current flow. In the DIFETs, a single gate voltage controls charge carriers of both polarities simultaneously. Depending upon configuration and geometry, DIFETs can enhance and/or deplete ambipolar current. Alternate embodiments are single injection FETs, which have charge carriers of only one polarity in the semiconductor body.

Vertical embodiments, called VMITs, are formed by successively depositing various layers. The gate is typically formed as a layer within the semiconductor body. The body is located between the two current electrodes. The gate layer has at least one opening through which the material of the current path extends. The gate may be formed as a Schottky barrier, or a reverse junction, or may be insulated. Certain VMITs feature multiple gates, and may be configured as AND, NOR or other logic gates.

Some DIFETs use space charge neutralization, achieved by a fourth electrode or other techniques, for even higher current, Enchancement mode DIFETs exhibit significant increased channel depth over an equivalent single carrier device. Some DIFETs, made preferably of amorphous silicon alloys, exhibit light emission. A DIFET laser made from such alloys is disclosed. Modulation of the ampiltude and/or frequency of the DIFET's optical output by varying gate voltage is disclosed.



ACTORUM AG